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ABSTRACT OF THE DISCLOSURE

Field effect transistor structures include a channel region formed in a recessed portion of a substrate. The recessed channel portion permits the use of relatively thicker source/drain regions thereby providing lower source/drain extension resistivity while maintaining the physical separation needed to overcome various short channel effects. The surface of the recessed channel portion may be of a rectangular, polygonal, or curvilinear shape. In a further aspect of the present invention, transistors are manufactured by a process in which a damascene layer is patterned, the channel region is recessed by etch that is self-aligned to the patterned damascene layer, and the gate electrode is formed by depositing a material over the channel region and patterned damascene layer, polishing off the excess gate electrode material and removing the damascene layer.

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